CLAIMS

I Claim:

1. A method of manufacturing a support circuit, comprising:

providing a conductive layer with top and bottom surfaces;

providing a top etch mask on the top surface that includes an opening that exposes a portion of the top surface;

providing a bottom etch mask on the bottom surface that includes an opening that exposes a portion of the bottom surface;

applying an etch to the exposed portion of the top surface through the opening in the top etch mask, thereby etching partially but not completely through the conductive layer and forming a recessed portion in the conductive layer below the top surface;

forming an insulative base on the recessed portion without forming the insulative base on the top surface;

applying an etch to the exposed portion of the bottom surface through the opening in the bottom etch mask, thereby forming a routing line in the recessed portion;

applying an etch to the insulative base to form an opening in the insulative base that exposes a portion of the recessed portion;

applying an etch to the exposed portion of the recessed portion through the opening in the insulative base, thereby forming an opening in the recessed portion with tapered sidewalls; and

providing an opening in the routing line using the opening in the recessed portion.

2. The method of claim 1, including providing the top and bottom etch masks simultaneously.

3. The method of claim 1, including providing the top and bottom etch masks during a single electroplating operation.

4. The method of claim 1, including removing the top and bottom etch masks simultaneously.

5. The method of claim 1, including applying the etch to the exposed portion of the top surface and then applying the etch to the exposed portion of the bottom surface.

6. The method of claim 1, including applying the etch to the exposed portion of the bottom surface and then applying the etch to the exposed portion of the recessed portion.

7. The method of claim 1, including providing the insulative base and then applying the etch to the exposed portion of the bottom surface.

8. The method of claim 1, including applying the etch to the exposed portion of the bottom surface and then forming the opening in the insulative base.

9. The method of claim 1, including applying the etch to the exposed portion of the top surface, then providing the insulative base, then applying the etch to the exposed portion of the bottom surface, then providing the opening in the insulative base, then applying the etch to the exposed portion of the recessed portion.

10. The method of claim 1, including applying an etch that enlarges the opening in the insulative base after forming the opening in the recessed portion.

11. The method of claim 10, wherein applying the etch that enlarges the opening in the insulative base exposes a portion of a top surface of the routing line adjacent to the tapered sidewalls and exposes an upper portion of the tapered sidewalls.

12. The method of claim 10, wherein applying the etch that enlarges the opening in the insulative base also at least partially forms an opening in an adhesive layer that is below the opening in the routing line.

13. The method of claim 10, including electroplating a metal onto the exposed portion of the top surface of the routing line and the tapered sidewalls before attaching the support circuit to a chip.

14. The method of claim 1, wherein the opening in the routing line has a diameter that increases with increasing height, and the tapered sidewalls have a slope of about 45 to 75 degrees.

15. The method of claim 1, wherein applying the etch to the exposed portion of the top surface forms a pillar in the conductive layer, and forming the insulative base allows the pillar to extend above the insulative base.

16. The method of claim 15, wherein the pillar has a diameter that is narrowest at the top surface.

17. The method of claim 15, wherein the routing line provides horizontal routing between the pillar and the opening in the routing line.

18. The method of claim 1, wherein applying the etches to the exposed portion of the top surface, the exposed portion of the bottom surface and the exposed portion of the recessed portion includes applying separate wet chemical etches, and applying the etch to the insulative base includes applying a laser etch.

19. The method of claim 1, wherein the conductive layer is a copper foil.

20. The method of claim 1, wherein the insulative base is epoxy.

21. A method of manufacturing a support circuit, comprising:

providing a conductive metal layer with top and bottom surfaces;

providing a top etch mask on the top surface and a bottom etch mask on the bottom surface, wherein the top etch mask includes an opening that exposes a portion of the top surface, and the bottom etch mask includes an opening that exposes a portion of the bottom surface;

applying an etch to the exposed portion of the top surface through the opening in the top etch mask, thereby etching partially but not completely through the conductive metal layer and forming a recessed portion in the conductive metal layer below the top surface;

forming an insulative base on the recessed portion that does not extend to the top surface;

applying an etch to the exposed portion of the bottom surface through the opening in the bottom etch mask, thereby forming a routing line in the recessed portion that is covered by the insulative base;

applying an etch to the insulative base for form an opening in the insulative base that exposes a portion of the routing line;

applying an etch to the exposed portion of the routing line through the opening in the insulative base to form an opening in the routing line with tapered sidewalls, wherein the opening in the routing line has a diameter which increases with increasing height, and a portion of a top surface of the routing line adjacent to an upper portion of the sloped sidewalls and the upper portion of the sidewalls are covered by the insulative base; and

applying an etch to the insulative base to enlarge the opening in the insulative base, wherein the enlarged opening in the insulative base exposes the portion of the top surface of the routing line and the upper portion of the sidewalls.

22. The method of claim 21, including providing the top and bottom etch masks simultaneously, and then removing the top and bottom etch masks simultaneously.

23. The method of claim 21, wherein the enlarged opening in the insulative base and the opening in the routing line provide a through-hole that extends through the support circuit.

24. The method of claim 21, including providing an adhesive beneath the routing line, wherein applying the etch that enlarges the opening in the insulative base also at least partially forms an opening in the adhesive directly beneath the opening in the routing line.

25. The method of claim 21, wherein the steps are performed in the sequence set forth.

26. The method of claim 21, wherein applying the etch to the exposed portion of the top surface forms a pillar in the conductive metal layer, and the routing line provides horizontal routing between the pillar and the opening in the routing line.

27. The method of claim 26, wherein the pillar is tapered and has a diameter that decreases as a height of the pillar increases and is narrowest at the top surface.

28. The method of claim 26, wherein the pillar extends a first distance above the routing line, the insulative base extends a second distance above the routing line, and the first distance is at least twice the second distance.

29. The method of claim 21, wherein the conductive metal layer is a copper foil.

30. The method of claim 21, wherein the insulative base is epoxy.

31. A method of manufacturing a support circuit, comprising the following steps in the sequence set forth:

providing a conductive metal layer with top and bottom surfaces;

providing a top etch mask on the top surface and a bottom etch mask on the bottom surface, wherein the top etch mask includes an opening that exposes a portion of the top surface, and the bottom etch mask includes an opening that exposes a portion of the bottom surface;

applying an etch to the exposed portion of the top surface through the opening in the top etch mask, thereby etching partially but not completely through the conductive metal layer, so as to form a pillar in the conductive metal layer that tapers and has a narrowest diameter at the top surface and form a recessed portion in the conductive metal layer below the top surface;

forming an insulative base on the recessed portion such that the pillar extends above the insulative base and the insulative base covers the recessed portion;

applying an etch to the exposed portion of the bottom surface through the opening in the bottom etch mask, thereby etching completely through the recessed portion to form a routing line in the recessed portion, and applying an etch to the insulative base to form an opening in the insulative base that exposes a portion of the routing line;

applying an etch to the exposed portion of the routing line through the opening in the insulative base to form an opening in the routing line with tapered sidewalls such that a diameter of the opening in the routing line increases as a height of the opening in the routing line increases and a portion of a top surface of the routing line adjacent to the tapered sidewalls is covered by the insulative base; and

applying an etch that enlarges the opening in the insulative base, wherein the enlarged opening in the insulative base exposes the portion of the top surface of the routing line adjacent to the tapered sidewalls.

32. The method of claim 31, including providing the top and bottom etch masks simultaneously, and then removing the top and bottom etch masks simultaneously.

33. The method of claim 31, including applying the etch to the exposed portion of the bottom surface and then applying the etch to the insulative base to form the opening in the insulative base that exposes the portion of the routing line.

34. The method of claim 31, including covering the bottom surface with an adhesive, and then applying the etch that enlarges the opening in the insulative base through the opening in the routing line to at least partially form an opening in the adhesive.

35. The method of claim 31, wherein the pillar extends a first distance above the routing line, the insulative base extends a second distance above the routing line, and the first distance is at least twice the second distance.

36. The method of claim 31, wherein the tapered sidewalls have a slope of about 45 to 75 degrees.

37. The method of claim 31, wherein the conductive metal layer is copper, and the insulative base is epoxy.

38. The method of claim 31, wherein the method excludes polishing.

39. The method of claim 31, wherein the support circuit is devoid of wire bonds, TAB leads, and solder joints.

40. The method of claim 31, wherein the support circuit is adapted for a semiconductor chip assembly.

41. A method of manufacturing a support circuit, comprising the following steps in the sequence set forth:

providing a copper layer with top and bottom surfaces;

providing a top etch mask on the top surface and a bottom etch mask on the bottom surface, wherein the top etch mask includes an opening that exposes a portion of the top surface, and the bottom etch mask includes an opening that exposes a portion of the bottom surface;

applying a wet chemical etch to the exposed portion of the top surface through the opening in the top etch mask, thereby etching partially but not completely through the copper layer, so as to form a pillar in the copper layer that extends to the top surface and a recessed portion in the copper layer below the top surface;

forming an insulative base on the recessed portion such that the pillar extends above the insulative base and the insulative base covers the recessed portion;

applying an etch to the exposed portion of the bottom surface through the opening in the bottom etch mask, thereby etching completely through the recessed portion, so as to form a routing line in the recessed portion that extends to the bottom surface and is covered by the insulative base, wherein the pillar extends a first distance above the routing line, the insulative base extends a second distance above the routing line, and the first distance is at least twice the second distance;

applying a wet chemical etch through an opening in the insulative base to form an opening in the routing line with tapered sidewalls such that a diameter of the opening in the routing line increases as a height of the opening in the routing line increases and a portion of a top surface of the routing line adjacent to an upper portion of the tapered sidewalls and the upper portion of the tapered sidewalls are covered by the insulative base; and

enlarging the opening in the insulative base such that the portion of the top surface of the routing line and the upper portion of the tapered sidewalls are directly beneath and exposed by the enlarged opening.

42. The method of claim 41, including applying a first laser etch to the insulative base to form the opening in the insulative base, and applying a second laser etch to the insulative base to form the enlarged opening in the insulative base.

43. The method of claim 42, including disposing an adhesive beneath the bottom surface, and applying the second laser etch through the opening in the insulative base and the opening in the routing line to at least partially form an opening in the adhesive, thereby providing a through-hole that consists of the enlarged opening in the insulative base, the opening in the routing line and the opening in the adhesive.

44. The method of claim 41, including electroplating a metal over the portion of the top surface of the routing line and the tapered sidewalls after enlarging the opening and before attaching the support circuit to a chip.

45. The method of claim 44, wherein the electroplated metal is adapted to receive a gold ball bond provided by wire bonding.

46. The method of claim 41, wherein the pillar has a flat top surface and a diameter that is narrowest at the flat top surface and a taper that extends from the flat top surface to the routing line.

47. The method of claim 41, wherein the tapered sidewalls have a slope of about 45 to 75 degrees.

48. The method of claim 41, wherein the method excludes polishing.

49. The method of claim 41, wherein the support circuit is devoid of wire bonds, TAB leads, and solder joints.

50. The method of claim 41, wherein the support circuit is adapted for a semiconductor chip assembly.

51. A support circuit adapted to be mechanically and electrically coupled to a semiconductor chip such that the support circuit and the chip in combination form a semiconductor chip assembly, the support circuit comprising:

an insulative base; and

a conductive trace embedded in the insulative base, wherein the conductive trace is a single continuous piece of metal, the conductive trace includes a pillar that extends above the insulative base and a routing line that is substantially covered by and extends below the insulative base, wherein an opening in the routing line has tapered sidewalls and a diameter that increases as height increases.

52. The support circuit of claim 51, wherein the insulative base includes an opening that exposes the opening in the routing line and a portion of a top surface of the routing line adjacent to the opening in the routing line.

53. The support circuit of claim 51, wherein the support circuit includes a through-hole that consists of the opening in the insulative base and the opening in the routing line.

54. The support circuit of claim 51, wherein the tapered sidewalls have a slope of about 45 to 75 degrees.

55. The support circuit of claim 51, wherein the pillar extends a first distance above the routing line, the insulative base extends a second distance above the routing line, and the first distance is at least twice the second distance.

56. The support circuit of claim 51, wherein the pillar has a flat top surface and a diameter that is narrowest at the top surface.

57. The support circuit of claim 56, wherein the pillar has a continuous taper between the top surface and the routing line.

58. The support circuit of claim 51, wherein the conductive trace is copper and the insulative base is epoxy.

59. The support circuit of claim 51, wherein the support circuit is devoid of wire bonds, TAB leads, and solder joints.

60. The support circuit of claim 51, wherein the semiconductor chip assembly is a chip size package.